Nonlinear Mixed Analysis/Optimization Algorithm for Microwave Power Amplifier Design

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Abstract—**A nonlinear mixed analysis/optimization algorithm for the design of microwave power amplifiers is presented. Matching conditions for optimum power and efficiency performance are imposed together with the balancing equations of the nonlinear analysis in a consistent way. The analysis/preoptimization of the power stage requires a computation time comparable to or smaller than a single conventional harmonic balance analysis. The algorithm forms the basis of a design procedure for the fulfilment of design specifications in terms of output power, power-added efficiency, and gain. Comparisons to the results of commercial CAD nonlinear analysis programs are presented.**

I. Introduction

CURRENTLY available methods for the design of microwave power amplifiers can be grouped into two broad categories: the "full nonlinear" and the "simplified quasi-nonlinear" ones.

To the first group belong, on one hand, the algorithms for the full nonlinear analysis of microwave circuits, based on complete nonlinear models for the active devices; and, on the other hand, the experimental techniques for the measurement of optimum load and source impedances under large-signal operating conditions. Nonlinear algorithms have been developed in the time domain [1], [2], in the frequency domain [3], [4], and in a mixed time-frequency domain [5]; they all require an accurate experimental modeling of the active component, and make use of sophisticated general-purpose computer programs now commercially available on most workstations [6]–[9]. Experimental techniques known as load/source pull are also now available to the designer thanks to dedicated equipment and software [10]–[12]: extensive measurements on the active device are automatically performed under large-signal drive for the complete characterization of the power stage.

The load/source pull technique is comparatively more straightforward, requires less skilled personnel and no preliminary modeling of the active device; the nonlinear simulation yields more informations on the electrical behavior of the stage, and allows greater flexibility (for instance, for harmonic control); moreover, the large-signal model can be used for other applications. Both require large and expensive equipments and considerable time effort: in both cases, in fact, the design is performed through repeated analyses or measurements until the optimum driving and loading conditions are obtained. In case the operating class must be optimized, the procedure must be repeated for each bias condition. Results are, however, usually accurate and reliable.

To the second group (the "simplified quasi-nonlinear" methods) belong techniques evaluating the optimum load line on the piecewise-linearized output characteristics of the (unidirectional) active device [13]–[16]; similar approaches including a more realistic model for the device, with internal feedback and parasitics [17]; waveform analysis techniques for the optimization of the harmonic content of the output waveforms [18]–[20]; and experimental procedures for the measurement of scattering parameters under large-signal drive, to be used in a conventional, linear way [21]. These methods, in various manners, make use of simplified models for the active component, and are also dedicated to the power analysis: they are therefore very fast. However, the inherent approximations reduce the accuracy of the results, quite often beyond the acceptable limits. On the other hand, their simplicity and speed make them very attractive for a preliminary investigation of power performances and design choices.

A technique combining the accuracy of full nonlinear analysis and the speed of dedicated optimization methods is therefore highly desirable.

In this paper, a mixed analysis/optimization algorithm using a nonlinear model of the active device is presented, dedicated to the design of microwave power amplifiers. "Matching" conditions for optimum power amplification are imposed at the same time and consistently with the solution of the nonlinear analysis: the values of matching elements in the circuit are also found as a result of the solution process. The computational effort required by the combined nonlinear circuit match and analysis is comparable to or even smaller than that of a single standard nonlinear analysis: matching equations replace part of the circuit analysis ones in the solving system. Since the nonlinear model and algorithm have no intrinsic approximations, the accuracy does not suffer any detriment.

The proposed method is the core of a design procedure involving the choice of operating class, drive level, and optimum loading of a power stage. Comparisons to results from a commercial CAD package show a major reduction in the computational effort. This method therefore proves to be suitable to a quick and accurate design of power amplifiers.

II. The Analysis Method

The basic assumptions, the resulting equations, and the numerical solving procedure of the proposed design-oriented

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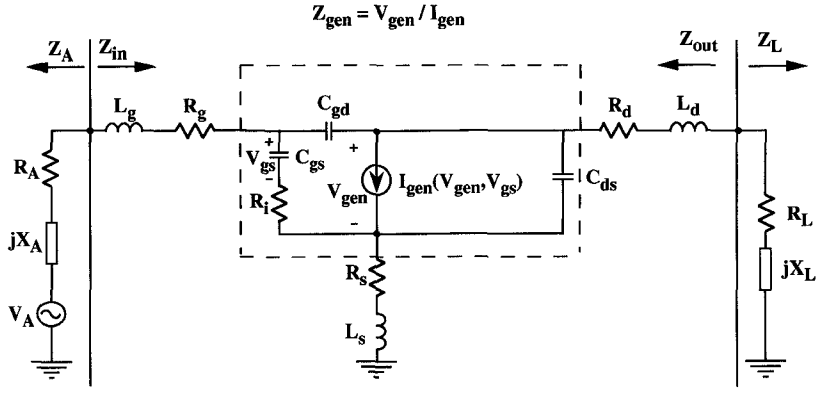

Fig. 1. Equivalent circuit model of the active device; intrinsic elements are boxed.

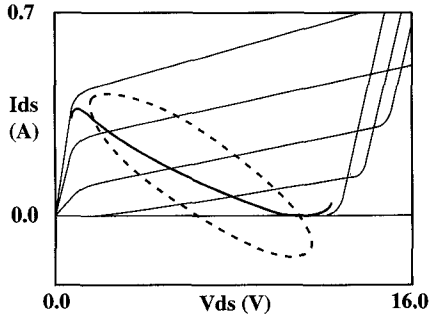

Fig. 2. Load curves superimposed on the output characteristics, measured at the intrinsic (solid line) and at the extrinsic (dashed line) drain terminal.

analysis/optimization method are described in detail in the following; fixed bias point and input power and also fixed resistive part of the load are assumed for the single analysis.

A. Assumptions and Conditions

Two basic hypotheses are made on the nonlinear power amplifier.

1) For high-power and high-efficiency operations, the load seen by the nonlinear voltage-controlled current source (Fig. 1) must be resistive [13], [14]. In fact, since the "hard" limits imposed by the output characteristics (i.e., breakdown, pinch-off, ohmic behavior, forward gate conduction, etc.) are the basic limitation to power generation, maximum active power is achieved when drain voltage and current are in-phase and their swings maximized: no hysteresis must be present in the load curve (i.e., the plot of instantaneous drain-source current versus drain-source voltage) and the load seen by the controlled current source must be therefore purely resistive. This condition is equivalent to resonating the reactive part of the load (as in [13]) only if some elements of the device's equivalent circuit (e.g., feedback elements as gate-drain capacitance and source inductance, or parasitics as drain inductance) are neglected. This condition is also clearly different from the standard conjugate match of a linear two-port, since the reactive currents must be compensated *at an internal port,* and the resistive load is determined by nonlinear limits (Fig. 2).

2) The nonlinear reactive elements of the device (i.e., the gate-source and gate-drain capacitances) can be replaced by bias-dependent linear equivalent elements when maximum power and efficiency evaluation is concerned. This hypothesis in fact is not, in the general case, required for the algorithm implementation, and has been introduced only for the sake of problem complexity reduction. Reactances do not contribute to power generation or dissipation, but only to waveform distortion and reactive power handling; in a well-designed amplifier, however, both effects are minimized and compensated by suitable matching at fundamental and harmonic frequencies (Fig. 3). The basic limitations of a power stage are due to the resistive (active) nonlinearities, i.e., mainly the voltage-controlled drain-source current source that is, therefore, the only nonlinear element in the equivalent circuit model used in the proposed analysis method (Fig. 1). Any general dependence of the drain current on gate-source and drain-source voltages is suitable, including nonquasi-static dispersion effects [22]–[24]; all other elements of the equivalent circuit model are present, including parasitic ones. As stated before, this second hypothesis could be removed using a complete nonlinear equivalent circuit, and a more general algorithm with the same characteristics developed; this simplification has been recognized to be a good compromise between speed and accuracy.

Under these hypotheses, a partial matching condition is thus imposed at the output of the device; a second condition of complete transfer of the power available at the input into the device is imposed, implying a conjugate match at the input port. It is important to note that the matching must be imposed under large-signal operations, i.e., with a large-signal fundamental-harmonic transconductance; this condition corresponds to the one that is obtained from a source-pull procedure. The matching at fundamental frequency is obtained through the tuning elements R_A, X_A, and X_L, while the resistive part of the load R_L is fixed, since it is a free design parameter.

Matching at harmonic frequencies too must contribute to produce a hysteresis-free load curve, i.e., a resistive load has to be seen by the nonlinear current generator at every harmonic. Any resistive harmonic termination, including short and open circuit, is allowed, and it is usually wise from a design point of view to choose it so that a proper wave-shaping at the output be achieved for design specifications fulfilment [18]; a free design parameter is therefore available at each harmonic frequency.

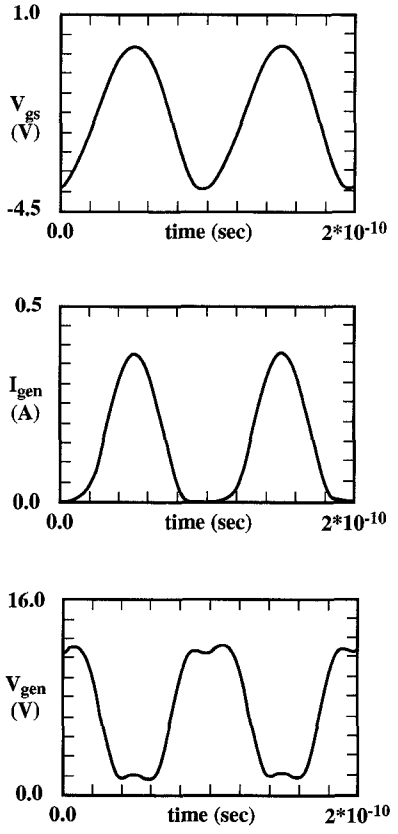

Fig. 3. (Top to bottom) Intrinsic gate-source voltage, drain-source voltage, and current versus time.

The additional constraint of waveform shaping at the input for maximum linearity and input reactance control, on the other hand, usually dictates some form of harmonic filters [25]; short circuits will be assumed here to minimize distortion, to prevent unwanted harmonic control voltages being generated by the harmonic currents that will occur at the input port.

B. The Nonlinear Equations

We recall that the analysis is performed for a fixed input power, bias point, and resistive part of the load. A standard harmonic balance analysis of the circuit requires the solution of a nonlinear system of equations. The fulfilment of the conditions described in the previous paragraph requires the solution of additional equations for large-signal circuit match; at the same time, however, it also reduces the number of harmonic-balancing nonlinear equations. In fact, at fundamental frequency, the (scalar) equation imposing the reactive part of the load $X_{gen}^{(1)}$ seen by the controlled current source to be zero forces the large-signal voltage and current to be in-phase; therefore, Kirchhoff's (harmonic-balancing) equation giving the large-signal amplitudes of voltage $V_{gen}^{(1)}$ and current $I_{gen}^{(1)}$ at the same port has now only a real part. The unknowns in the two equations are the reactive matching element in the output network $X_{Load}^{(1)}$, the matching elements in the input network Z_A and the amplitude of the internal drain-source voltage $V_{gen}^{(1)}$:

$$X_{gen}^{(1)} = X_{gen}^{(1)}(X_{Load},\, Z_A,\, g_{m,\,LS}) = 0 \qquad (1)$$

$$V_{gen}^{(1)} - R_{gen}^{(1)} \cdot I_{gen}^{(1)} = V_{gen}^{(1)} - R_{gen}^{(1)}(X_{Load},\, Z_A,\, g_{m,\,LS}) \cdot I_{gen}^{(1)}(X_{Load},\, Z_A,\, V_{gen}) = 0. \qquad (2)$$

The intrinsic drain current harmonic components $I_{gen}^{(n)}$ (Fig. 1) are computed from the drain-source and gate-source voltage through a time-domain integration and Fourier transform as in the standard harmonic-balance procedure. The two equations are coupled through the large-signal transconductance, defined as

$$g_{m,\,LS} = \frac{\partial I_{gen}^{(1)}(X_L,\, Z_A,\, V_{gen})}{\partial V_{gs}(X_L,\, Z_A,\, V_{gen})}.$$

The additional complex equation imposing complex conjugate match at the input has to be added:

$$Z_A = Z_{in}^{*}(X_{load},\, g_{m,\,LS}) \qquad (3)$$

equivalent to the couple of scalar equations

$$R_A = \mathrm{Re}\,[Z_{in}(X_{Load},\, g_{m,\,LS})]$$
$$X_A = -\mathrm{Im}\,[Z_{in}(X_{Load},\, g_{m,\,LS})].$$

Among the four resulting scalar equations, however, only (2) requires the costly time-domain integration and Fourier transform of the standard harmonic-balance procedure; the other three are simple frequency-domain matching equations incorporating the large-signal transconductance $g_{m,\,LS}$. When the system of four coupled scalar nonlinear equations is solved, a combination of partial load and source pulling and of nonlinear analysis is simultaneously and consistently achieved; only the load resistance is *a priori* fixed as a free design parameter, as already stated.

One "matching" and one "harmonic balancing" Kirchhoff's equation at the *internal drain-source port* must similarly be added for each harmonic frequency. The additional unknowns are a (frequency selective) reactive matching element in the output network and the real amplitude of the drain-source voltage harmonic component for each frequency; no input match is obviously required. At dc, only a scalar balancing equation must be solved. The complete system is therefore

$$\begin{aligned}
V_{gen}^{(0)} - R_{gen}^{(0)} \cdot I_{gen}^{(0)} &= 0 \text{(scalar)(bias conditions+rectification)} \\
Z_A &= Z *_{in} \text{(complex)(large-signal input math)} \\
X_{gen}^{(1)} &= 0 \text{(scalar)(match at the current source)} \\
V_{gen}^{(1)} - R_{gen}^{(1)} \cdot I_{gen}^{(1)} &= 0 \text{(scalar)(harmonic balance)} \\
&\vdots \\
X_{gen}^{(n)} &= 0 \text{(scalar)(match at the current source)} \\
V_{gen}^{(n)} - R_{gen}^{(n)} \cdot I_{gen}^{(n)} &= 0 \text{(scalar)(harmonic balance)}
\end{aligned} \qquad (4)$$

where $V_{gen}^{(n)}$ and $I_{gen}^{(n)}$ are the amplitudes of the nth harmonic of the intrinsic drain-source voltage and current, respectively, and $R_{gen}^{(n)}$ and $X_{gen}^{(n)}$ are the real and imaginary part of the load seen from the current source at the nth harmonic frequency.

Solving this system leads to imposing large-signal matching conditions suitable for power amplification, and to simultaneously and consistently finding the nonlinear voltages and currents relative to this partially optimized circuit.

C. The Solving Procedure

As stated before, the system includes nonlinear equations relative to the "matching" of the linear network: they impose the large-signal load of the nonlinear current source to be resistive and large-signal input match. It also includes nonlinear equations imposing the "balancing" of the harmonic coefficients at the port connecting the linear and nonlinear subnetworks (the intrinsic drain-source port).

The first kinds of equations are written in the frequency domain, and the only link with the "harmonic balancing" equations is the large-signal transconductance at the corresponding harmonic frequency, used in the "matching" expressions. They are nonlinear because the unknowns to be determined are tuning elements (Z_A, $X_{gen}^{(n)}$), that appear in an elaborated way inside the equations; however, they can be solved very quickly with simple iterative algorithms (e.g., fixed point).

The "harmonic balancing" equations, on the other hand, require a time-consuming time-domain waveform computation and Fourier transform in order to find the spectral coefficients of the current of the nonlinear element. It is worth noting that half of the time domain current waveform samples are needed for the Fourier transform: only the magnitudes must be found, since the phases are zero due to the absence of hysteresis in the load curve.

In the proposed procedure, the two kinds of equations are alternately and iteratively solved until a simultaneous and consistent solution is reached; the first guess is taken from a previous analysis result, or from a linear analysis if no guess is available, as usual in nonlinear algorithms. Convergence is faster than in the case of a standard harmonic balance problem: the number of equations is nearly the same (only the input matching equations are added), but the "balancing" equations have twice-as-fast Fourier transform, and the "matching" equations, which constitute half of the system, have an extremely fast solution. Only a few seconds are required on a 80486 PC to reach convergence in a typical case.

As an example, in Fig. 4, output power, large-signal gain, and power-added efficiency, computed with the proposed method (solid line), are plotted versus input power and compared to the results of a commercial CAD program ([7], dotted): the minor discrepancies between the two methods arise from the use of linear reactances in the proposed method. The device used is a GEC Marconi B2 medium power MESFET, whose equivalent circuit model [26] has been extracted using both pulsed dc measurements and RF small-signal S-parameters at multiple bias points. It must be stressed that the results of the commercial software package are obtained performing a simulated load/source pull for each input power, and the plots in Fig. 4 are therefore not standard power sweeps. The time needed to obtain such plots with the proposed approach is substantially smaller (more than one order of magnitude, with a nonoptimized code) than that required for the simulated load/source pull.

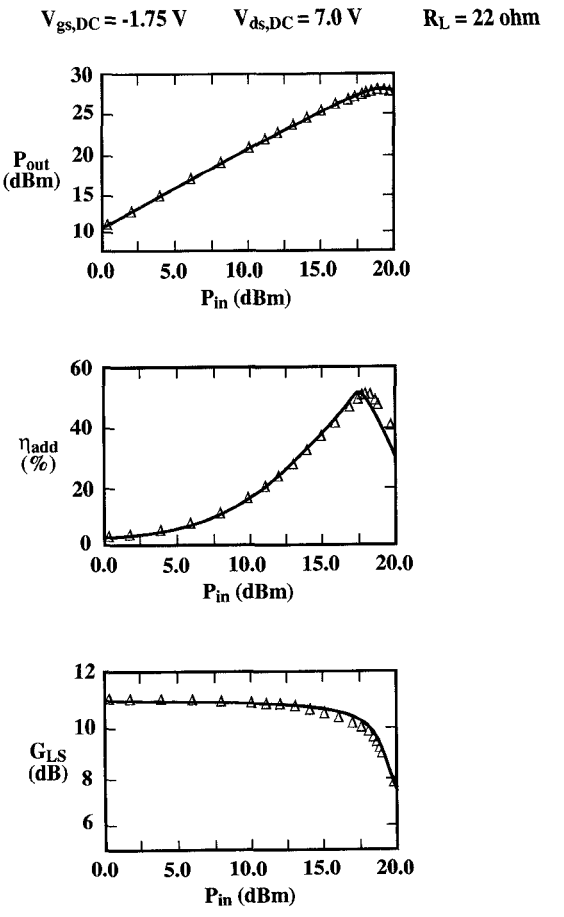

Fig. 4. (Top to bottom) Output power, power-added efficiency, and large-signal gain versus input power computed with the proposed method (solid) and with a commercial CAD program ([7], symbols).

III. The Design Method

We briefly review the method. The algorithm does not simply analyze a real-world circuit as it is, leaving the optimization to the designer's ability: it is a mixed analysis/optimization procedure. For a given bias point, drive level, and load resistance, the optimum large-signal complex input match and reactive output match are imposed, and the performances of this "partially optimized" stage are computed in a substantially shorter time than a single standard nonlinear analysis. The method is therefore suitable for a systematic investigation and optimization of bias point, load, and drive level, which cannot be automatically found: rather, they are a designer's choice, subject to design compromises.

The choice of the optimum bias point (i.e., the pair of bias voltages $V_{gs,\,DC}$ and $V_{ds,\,DC}$) depends on the design specifications: if, for instance, a low-voltage design is concerned, the drain bias voltage is fixed, leaving the gate bias alone (i.e., the operating class) as a designer's choice. Similarly, if the output power must be maximized, it is usually wise to choose the drain bias voltage so to maximize the output waveforms swings; the drain bias voltage can therefore be selected according to [27]

$$V_{ds,\,DC} = \frac{V_{br,\,po} - V_{po} - V_{bi} - 2|V_{gs,\,DC}| + V_k}{2}$$

where $V_{br,\,po}$ is the drain-source breakdown voltage for $V_{gs} = V_{po}$ (gate-source pinch-off voltage), V_{bi} is the built-in voltage of the gate-source junction, and V_k is the knee voltage. A

single parameter (the operating class) is therefore assumed in the following as a free bias parameter to be optimized.

The reactive parts of the fundamental and harmonic load terminations come out of the analysis/optimization process, as stated above. The selection of the resistive parts, on the other hand, requires some care: they can be used to match, as much as possible, design specifications if a "maximum efficiency" or "maximum power" design is concerned [18]; however, if the complexity of the harmonic-terminating circuitry is too high, or if the harmonic terminations cannot effectively be controlled at such high frequencies, a good compromise which has been recognized is to short all harmonic frequencies [15], [27]. In fact, the output capacitive reactance of the active device usually dominates at higher frequencies, acting as a short circuit. Moreover, this choice leads to a great simplification of the design procedure, and allows a major reduction of the number of equations to be solved: in this case, the system (4) reduces to

$$\begin{aligned} DC \quad & V_{gen}^{(0)} - R_{gen}^{(0)} \cdot I_{gen}^{(0)} = 0(\text{scalar}) \\ & Z_A = Z_{in}^{*} \qquad (\text{complex}) \\ f_0 \quad & X_{gen}^{(1)} = 0(\text{scalar}) \\ & V_{gen}^{(1)} - R_{gen}^{(1)} \cdot I_{gen}^{(1)} = 0(\text{scalar}). \end{aligned}$$

The resistive part of load at the fundamental frequency only is therefore assumed in the following as a second free parameter to be optimized.

The third free parameter, i.e., the drive level, can be chosen through a suitable condition. When a single analysis is finished, output power P_{out}, large-signal power gain G_{LS}, and power-added efficiency η_{add} are immediately available:

$$P_{DC} = I_{ds}^{(0)} \cdot V_{ds}^{(0)} \qquad P_{out} = \frac{V_{ds}^{(1)} \cdot I_{ds}^{(1)}}{2} \qquad G_{LS} = \frac{P_{out}}{P_{in}}$$

$$\eta_{add} = \frac{P_{out} - P_{in}}{P_{DC}}.$$

For a given bias point and load, the input level can be swept from linear to saturated behavior, and the point of interest selected depending on the design specifications; possible alternatives are the 1-dB gain compression point, the maximum efficiency point, or the saturated output power point. It must be noted that this procedure (source stepping) has also the well-known advantage of easing the nonlinear analysis: starting from the linear solution for the first low-level point, the solution of the previous point is used as the first guess for the algorithm for any input power. This method greatly speeds up the solution, and allows a careful selection of the drive level.

In this way, only two free design parameters are now left: operating class and resistive part of the load at fundamental frequency. The proposed design procedure is based on the preliminary calculation of tables or plots of the output quantities (P_{out}, G_{LS}, η_{add}) through repeated analyses within a certain range of values of the free design parameters. Bias point (or drain-source quiescent current) is swept from class B to class A, and for each bias the load resistance is varied within a suitable range. For each pair of values, the input power is selected corresponding, in this case, to the point of maximum efficiency, as explained above. The results for a Plessey P1135 medium power MESFET are shown in Fig. 5 (connected symbols) as functions of the load resistance, with the quiescent current as a parameter. In the same plots, results from a commercial CAD program ([6], disconnected symbols) are shown for comparison. The two methods are in substantial agreement, but the proposed one required about one order of magnitude less computer time.

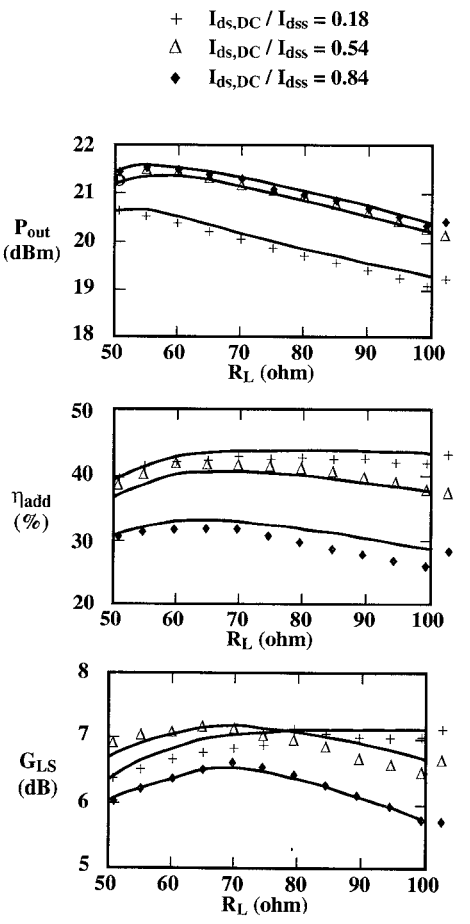

Fig. 5. (Top to bottom) Output power, power-added efficiency, and large-signal gain versus resistive part of the load, with the quiescent current as a parameter, with the proposed method (solid line), and with a commercial CAD program ([6], symbols).

In Fig. 6, results for the previously described GEC Marconi B2 power MESFET are also shown. It is easily seen that it is not possible to simultaneously maximize output power, gain, and efficiency, as expected. In fact, holding the load constant and considering the variation of the output quantities with the class of operation, dc power consumption beneficially decreases moving toward class B. Nevertheless, at the same time, output power and gain decrease: a point of maximum efficiency is usually present in class AB as a result of these contrasting effects.

On the other hand, for certain choices of the operating class, increasing the load resistance beyond the value corresponding to the point of maximum output power may result in a further increase of the power-added efficiency. This particular behavior is due to the increase of the large-signal gain compensating the decrease of the drain efficiency, and it is typical of low-gain

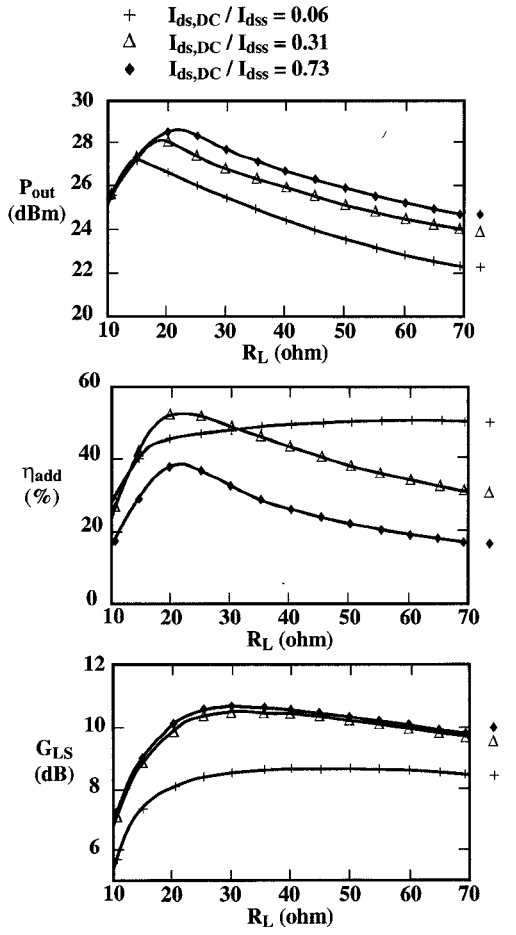

Fig. 6. Output power, power-added efficiency and large-signal gain, versus resistive part of the load, with the quiescent current as a parameter.

operating conditions (near class-B and/or at high frequencies). A compromise must then be accepted by the designer.

The analysis/optimization process can be exploited in other ways. In some applications, the choice of the operating class is forced by minimum dc power dissipation (i.e., class-B) or maximum dynamic range (i.e., class A) requirements; in this case, the free parameters are only the drive level and the load resistance. A quantitative tradeoff, corresponding to the operating compression or backoff level and loading, must be found between maximum power and maximum efficiency conditions. For this purpose, in Fig. 7 constant output power and power-added efficiency contours are plotted as functions of the resistive part of the load and input power for a given bias condition. Maximum efficiency and maximum power points are not in the same region, but allow the designer to tradeoff between the two optima, selecting the desired operating condition.

IV. Conclusion

A nonlinear mixed analysis/optimization algorithm has been presented for the design of microwave power amplifiers. Matching conditions for maximum power and efficiency performance are imposed together with the balancing equations of the nonlinear analysis in a consistent way. The algorithm therefore performs a partial source- and load-pull, yielding a

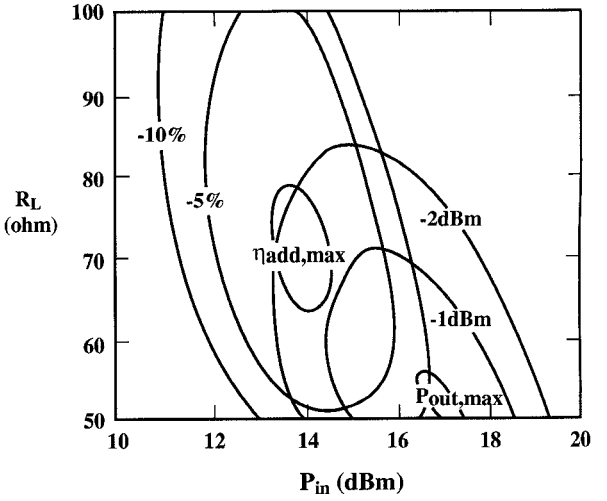

Fig. 7. Constant output power and power-added efficiency contours in the load/input power plane.

preoptimized power stage; the computational effort, however, is smaller than that of a single standard nonlinear analysis.

The proposed method can be used as the core of a design procedure investigating the possible tradeoff among operating class, drive level, and optimum loading of the power stage. Comparisons to results from a commercial CAD package show a major reduction in the computational effort without substantial loss of accuracy. The proposed method therefore proves to be suitable for a quick and accurate design of power amplifiers, and an advantageous and flexible alternative to existing design procedures.

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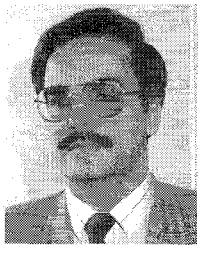
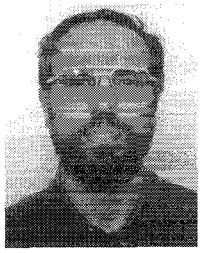


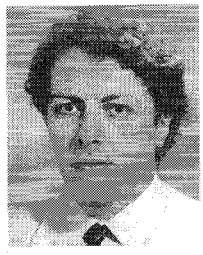
Franco Giannini was born in Galatina (LE), Italy, in 1944. He received the degree in electronic engineering from the University of Roma "La Sapienza," Italy, in 1968.

He was a research assistant at the University of Roma "La Sapienza," an associate professor at the University of Ancona, and is currently a full professor of Applied Electronics at the University of Roma "Tor Vergata." His main fields of interest are microwave planar passive components characterization and modeling, GaAs technology, and active MMIC design (both linear and nonlinear).



Giorgio Leuzzi received the degree in electronic engineering from the University of Roma "La Sapienza," Italy, in 1982.

He served in the Italian Army as an officer in the Technical Corps in 1983. In 1984 he became a research assistant at the University of Roma "Tor Vergata." Since 1991 he has taught microwave electronics at the same university. He worked in the field of microwave integrated transmission lines and is now involved in the study of nonlinear microwave circuits. His main interests are physical device modeling, nonlinear circuit analysis, and active circuit design.



Ernesto Limiti was born in Roma, Italy, on March 26, 1965. He received the degree in electronic engineering from the University of Roma "Tor Vergata," Italy, in 1989.

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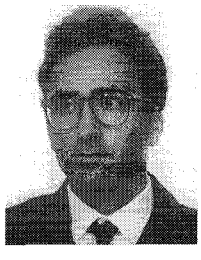

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